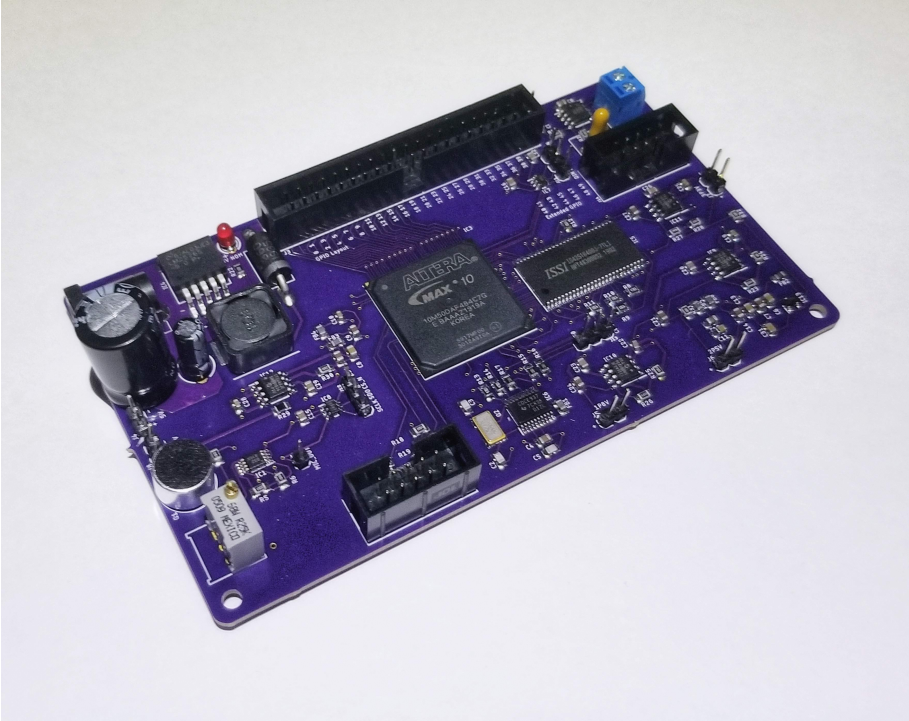
Max 10 Pollen Board User Manual



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Chapter 1

Introduction

The Max 10 Pollen Board is a FPGA design development board centered around the Altera MAX 10 FPGA with a focus on digital signal processing. When you need high-volume applications, including protocol bridging, motor control drive, analog to digital conversion, image processing, and handheld devices, the MAX 10 Lite FPGA is your best choice.

The Max 10 Pollen Board includes hardware such an integrated electret microphone, SPI enabled Analog to Digital Converter, 16MB SDRAM, SPI Enabled Digital to Analog Converter, an audio amplifier, and more. All of these capabilities make the Max 10 Pollen Board an excellent choice for digital audio processing development on the powerful Altera MAX 10 FPGA.

The Max 10 Pollen Board is meant to be programmed over Altera's JTAG programmer the USB Blaster.

1.1 Layout and Components

This section presents the features and design characteristics of the board. The photographs of the board shown in Figure 1.1 and Figure 1.2 depicts the layout of the board and indicates the location of key components.

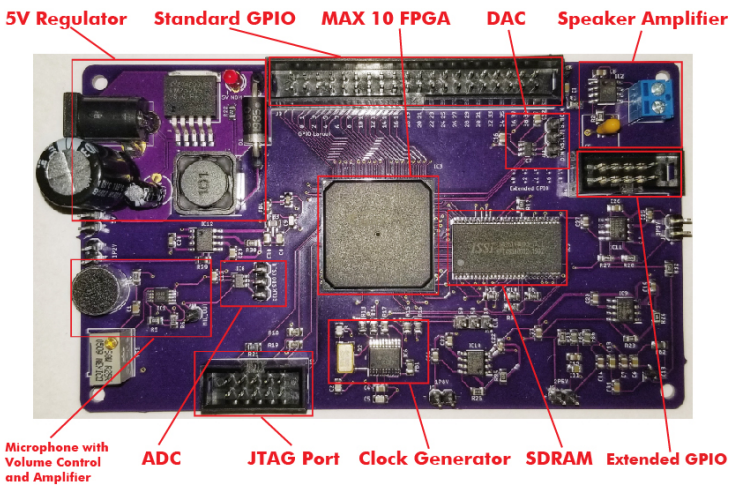

Figure 1.1: Max 10 Pollen Board - Top View

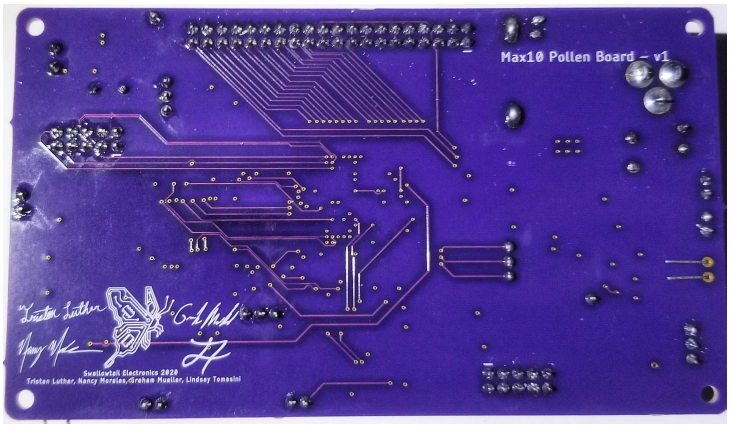

Figure 1.2: Max 10 Pollen Board - Bottom View

The following hardware is provided on the board:

1.1.1 ALTERA Max 10

- MAX 10 10M50DAF484C7G Device
- Integrated dual ADCs, each ADC supports 1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1,638 Kbits M9K Memory
- 5,888 Kbits user flash memory
- 144 18 18 Multiplier

- 4 PLLs (Phase Locked Loop)

1.1.2 Memory Device

- IS42S16400J-7TLI 64MB SDRAM x16 bits data bus

1.1.3 GPIO Connectors

- 2x20 Shrouded GPIO Header
- 2x5 Shrouded GPIO Header

1.1.4 Instrumentation Amplifier & Microphone

- INA332AIDGKR Instrumentation Amplifier
- Electret Microphone (2.2k Ohm)

1.1.5 Analog to Digital Converter

- ADS7868IDBVR 8-bit SPI Analog to Digital Converter

1.1.6 Speaker Amplifier & Expected Impedance

- LM4991MAX Speaker Amplifier
- Output speaker can be from 4-12 Ohm.

1.1.7 Digital to Analog Converter

- AD5320BRTZ-REEL7 12-bit SPI Digital to Analog Converter

1.1.8 Power

- 5VDC - 12VDC input from 2.1mm Barrel Jack Connector
- LM2576HVS 5V Fixed Buck Converter
- 4x MCP1726T-ADJE Linear

1.2 Block Diagram of the Board

Figure 1.3 gives the block diagram of the board. To provide ease of use, all connections are made though the MAX 10 FPGA. Thus, the user can configure the FPGA to implement their system designs.

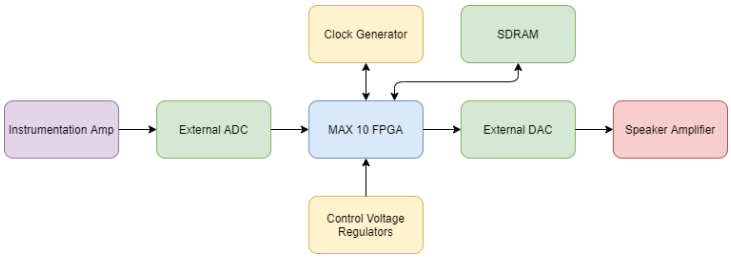

Figure 1.3: Board Block Diagram

1.3 Programming the Board

Configuration and programming of the board is recommend to be done though the Quartus Prime software suite. The Max 10 Pollen Board features a 2x5 Shrouded Connector that functions as a JTAG programming port (See Figure 1.1). The Altera USB Blaster JTAG programming device is meant to be connected to this port for configuration and programming. A demonstration of this connections is shown in Figure 1.4.

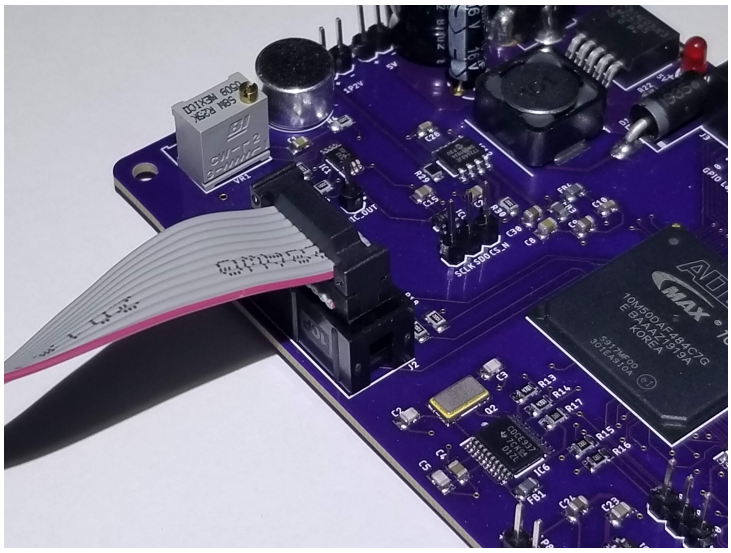

Figure 1.4: USB Blaster Connection

Chapter 2

Using the Pollen Board

The Max 10 Pollen Board FPGA GPIO pins can be configured though the 'Pin Planner' in Quartus Prime. See Figure 2.1. The Pin Planner can also be reached with the shortcut 'CTRL+SHIFT+N'.

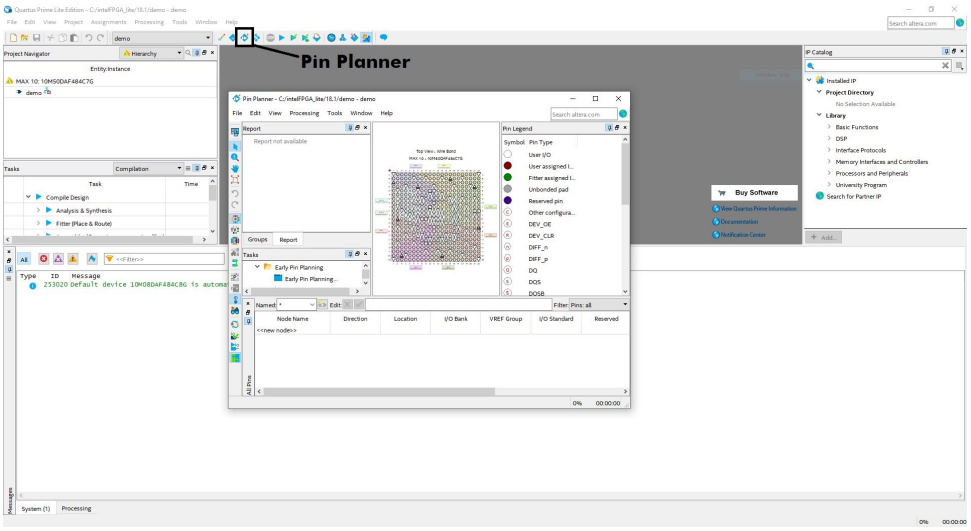

Figure 2.1: Pin Planner Location in Quartus

From here the pins of the FPGA can be configured for the HDL file containing your program. The following sections of this chapter will describe the pinouts of the hardware available for interaction with the FPGA. The pinouts go as follows:

2.1 Controlling Clock Circuitry

The Texas Instruments CDCE937PWR Programmable 3-PLL VCXO Clock Synthesizer is used to generate a clock signal for the MAX 10 FPGA. The two 50MHz clock signals connected to the FPGA are used as sources for user logic. The 10MHz clock signal is connected to PPL1 and PLL3 of the FPGA, the outputs of these two PLLs can drive the ADC clock. The pin assignment for clock inputs is listed in Table 2.1.

Table 2.1: Clock Circuity Pin Assignment

Signal Name	FPGA Pin No.	Description	I/O Standard
ADC_CLK_10	PIN_N5	10 MHz input for ADC (Internal)	3.3-V LVTTL
MAX10_CLK1_50	PIN_P11	50 MHz clock input	3.3-V LVTTL
MAX10_CLK2_50	PIN_N14	50 MHz clock input	3.3-V LVTTL

2.2 Controlling GPIO

There are 40 standard GPIO pins though the 2x20 shrouded header connector. Each of these header pins is connected directly to the MAX 10 FPGA.

Figure 2.2 shows the related schematics. Table 2.2 shows the pin assignment.

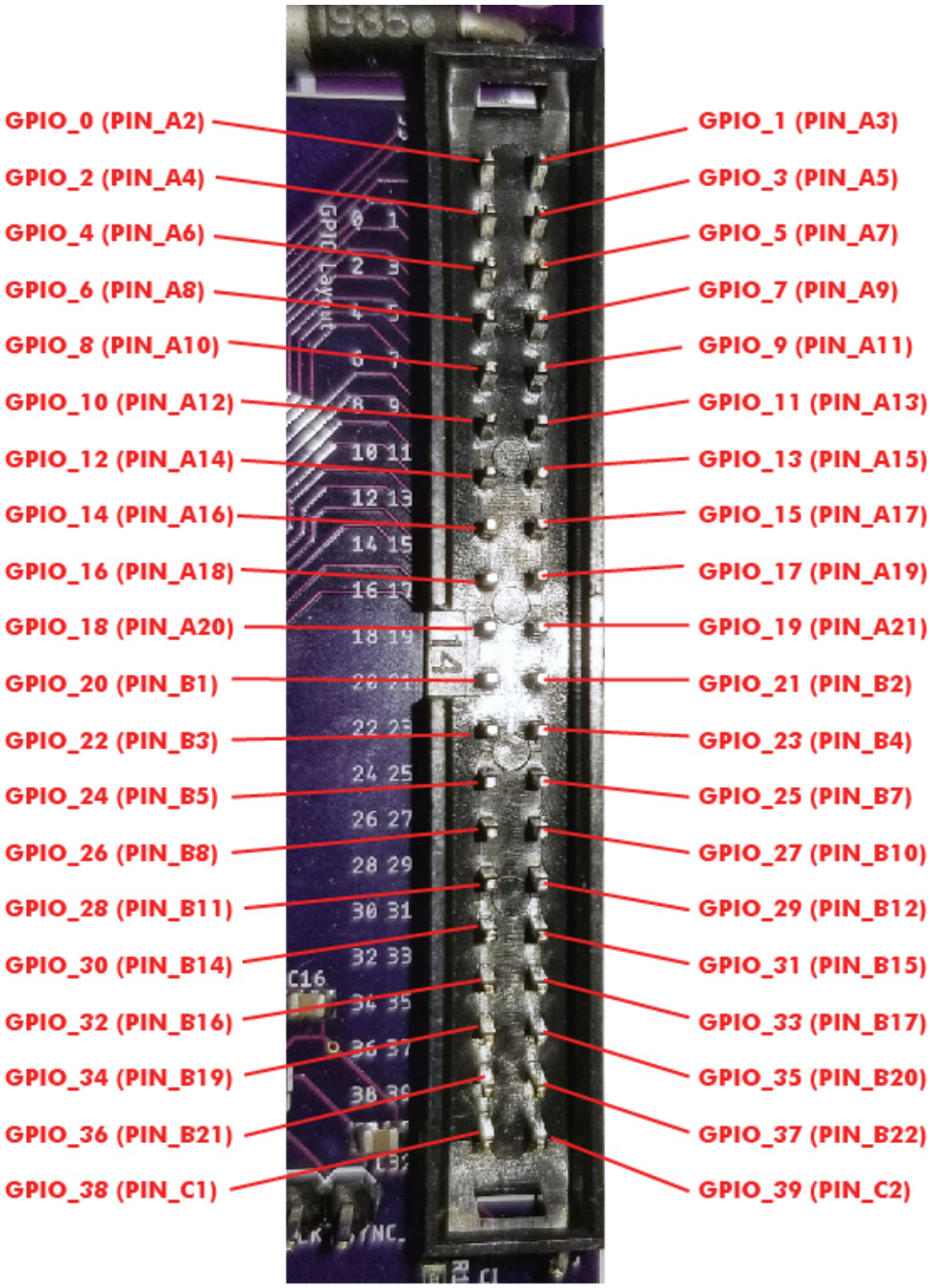

Figure 2.2: Standard I/O location on hardware

Table 2.2: Standard GPIO Pin Assignment

Signal Name	FPGA Pin No.	Description	I/O Standard
GPIO_0	PIN_A2	GPIO Connection [0]	3.3-V LVTTL
GPIO_1	PIN_A3	GPIO Connection [1]	3.3-V LVTTL
GPIO_2	PIN_A4	GPIO Connection [2]	3.3-V LVTTL
GPIO_3	PIN_A5	GPIO Connection [3]	3.3-V LVTTL
GPIO_4	PIN_A6	GPIO Connection [4]	3.3-V LVTTL
GPIO_5	PIN_A7	GPIO Connection [5]	3.3-V LVTTL
GPIO_6	PIN_A8	GPIO Connection [6]	3.3-V LVTTL
GPIO_7	PIN_A9	GPIO Connection [7]	3.3-V LVTTL
GPIO_8	PIN_A10	GPIO Connection [8]	3.3-V LVTTL
GPIO_9	PIN_A11	GPIO Connection [9]	3.3-V LVTTL
GPIO_10	PIN_A12	GPIO Connection [10]	3.3-V LVTTL
GPIO_11	PIN_A13	GPIO Connection [11]	3.3-V LVTTL
GPIO_12	PIN_A14	GPIO Connection [12]	3.3-V LVTTL
GPIO_13	PIN_A15	GPIO Connection [13]	3.3-V LVTTL
GPIO_14	PIN_A16	GPIO Connection [14]	3.3-V LVTTL
GPIO_15	PIN_A17	GPIO Connection [15]	3.3-V LVTTL
GPIO_16	PIN_A18	GPIO Connection [16]	3.3-V LVTTL
GPIO_17	PIN_A19	GPIO Connection [17]	3.3-V LVTTL
GPIO_18	PIN_A20	GPIO Connection [18]	3.3-V LVTTL
GPIO_19	PIN_A21	GPIO Connection [19]	3.3-V LVTTL
GPIO_20	PIN_B1	GPIO Connection [20]	3.3-V LVTTL
GPIO_21	PIN_B2	GPIO Connection [21]	3.3-V LVTTL
GPIO_22	PIN_B3	GPIO Connection [22]	3.3-V LVTTL
GPIO_23	PIN_B4	GPIO Connection [23]	3.3-V LVTTL
GPIO_24	PIN_B5	GPIO Connection [24]	3.3-V LVTTL
GPIO_25	PIN_B7	GPIO Connection [25]	3.3-V LVTTL
GPIO_26	PIN_B8	GPIO Connection [26]	3.3-V LVTTL
GPIO_27	PIN_B10	GPIO Connection [27]	3.3-V LVTTL
GPIO_28	PIN_B11	GPIO Connection [28]	3.3-V LVTTL
GPIO_29	PIN_B12	GPIO Connection [29]	3.3-V LVTTL
GPIO_30	PIN_B14	GPIO Connection [30]	3.3-V LVTTL
GPIO_31	PIN_B15	GPIO Connection [31]	3.3-V LVTTL
GPIO_32	PIN_B16	GPIO Connection [32]	3.3-V LVTTL
GPIO_33	PIN_B17	GPIO Connection [33]	3.3-V LVTTL
GPIO_34	PIN_B19	GPIO Connection [34]	3.3-V LVTTL
GPIO_35	PIN_B20	GPIO Connection [35]	3.3-V LVTTL
GPIO_36	PIN_B21	GPIO Connection [36]	3.3-V LVTTL
GPIO_37	PIN_B22	GPIO Connection [37]	3.3-V LVTTL
GPIO_38	PIN_C1	GPIO Connection [38]	3.3-V LVTTL
GPIO_39	PIN_C2	GPIO Connection [39]	3.3-V LVTTL

2.3 Controlling Extended GPIO

There are 10 extended GPIO pins though the 2x5 shrouded header connector. Each of these header pins is connected directly to the MAX 10 FPGA.

Figure 2.3 shows the related schematics. Table 2.3 shows the pin assignment.

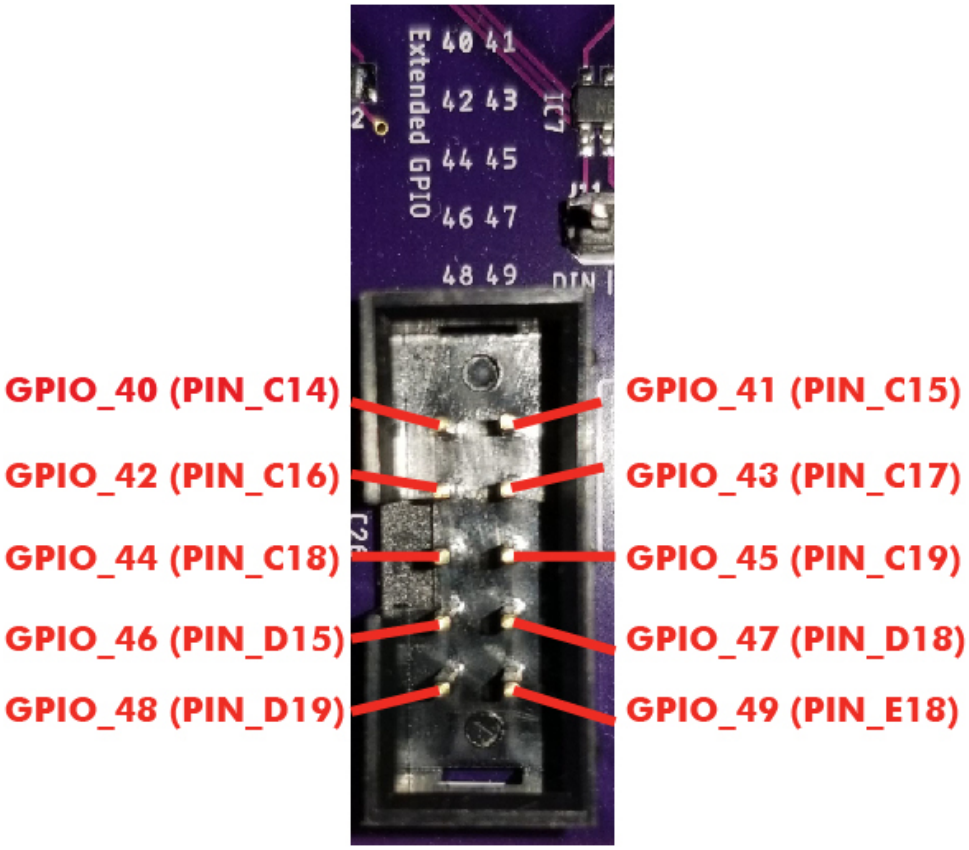

Figure 2.3: Extended I/O location on hardware

Table 2.3: Standard GPIO Pin Assignment

Signal Name	FPGA Pin No.	Description	I/O Standard
GPIO_40	PIN_C14	GPIO Connection [40]	3.3-V LVTTL
GPIO_41	PIN_C15	GPIO Connection [41]	3.3-V LVTTL
GPIO_42	PIN_C16	GPIO Connection [42]	3.3-V LVTTL
GPIO_43	PIN_C17	GPIO Connection [43]	3.3-V LVTTL
GPIO_44	PIN_C18	GPIO Connection [44]	3.3-V LVTTL
GPIO_45	PIN_C19	GPIO Connection [45]	3.3-V LVTTL
GPIO_46	PIN_D15	GPIO Connection [46]	3.3-V LVTTL
GPIO_47	PIN_D18	GPIO Connection [47]	3.3-V LVTTL
GPIO_48	PIN_D19	GPIO Connection [48]	3.3-V LVTTL
GPIO_49	PIN_E18	GPIO Connection [49]	3.3-V LVTTL

2.4 Controlling ADC

The Texas Intruments ADS7868IDBVR 8-bit SPI Analog to Digital converter has its outputs directly wired to the MAX 10 FPGA. The ADC expects an analog signal ranging between 0 -

3.3V. The analog signal is on the node labeled MIC_OUT and is directly wired the output of the instrumentation amplifier of the microphone. The input is also addressable from the labeled header pin (See Figure 2.4).

Figure 2.4 shows the related schematic. Table 2.4 shows the pin assignment.

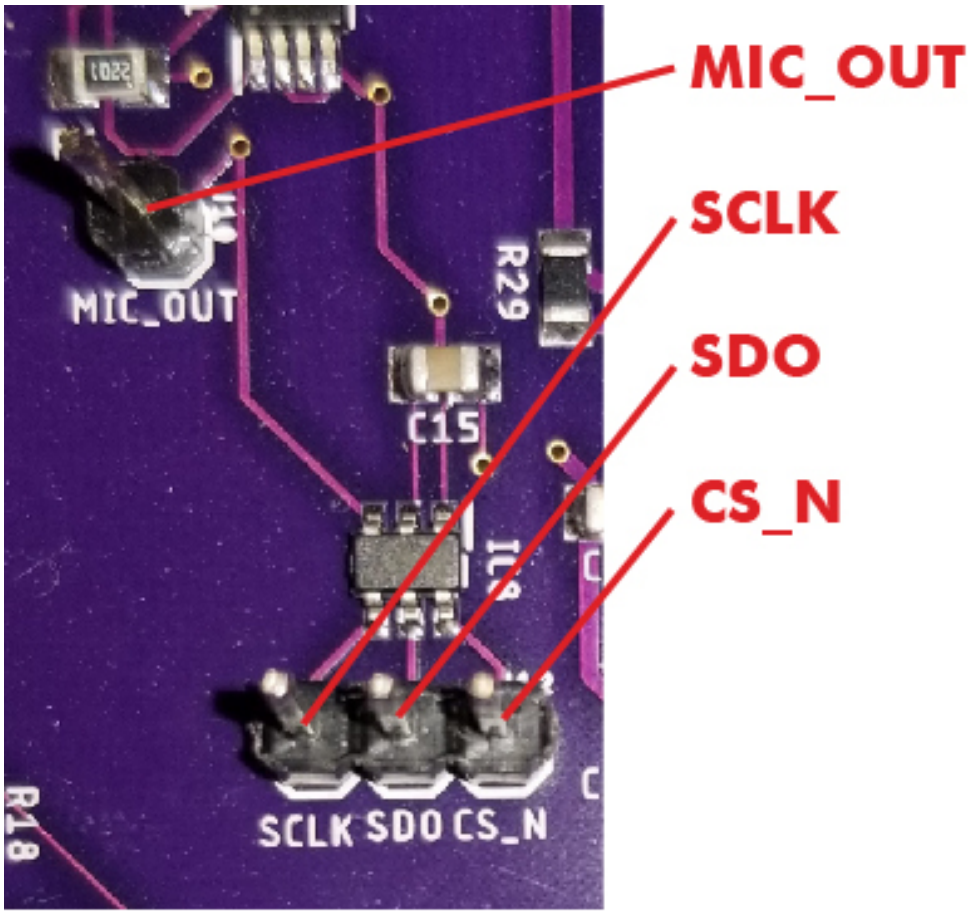

Figure 2.4: External ADC on hardware

Table 2.4: External ADC Pin Assignment

Signal Name	FPGA Pin No.	Description	I/O Standard
CS_N_ADC	PIN_W1	SPI Slave Select Line for ADC	3.3-V LVTTL
SDO_ADC	PIN_Y1	SPI Data Line for ADC	3.3-V LVTTL
SCLK_ADC	PIN_AA1	SCLK for SPI clock input	3.3-V LVTTL

2.5 Controlling DAC

The Analog Device AD5320BRTZ-REEL7 12-bit SPI Digital to Analog converter has its inputs directly wired to the MAX 10 FPGA. The analog signal output is on the node labeled J9 and is directly wired the input of the speaker amplifier. The input is also addressable from the labeled

header pin (See Figure 2.5).

Figure 2.5 shows the related schematic. Table 2.5 shows the pin assignment.

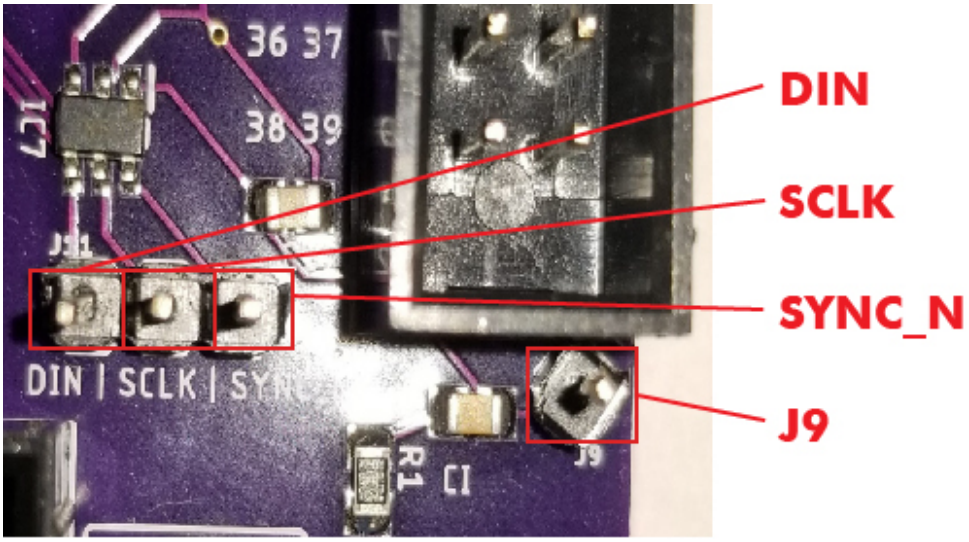

Figure 2.5: External DAC on hardware

Table 2.5: External DAC Pin Assignment

Signal Name	FPGA Pin No.	Description	I/O Standard
SYNC_N_DAC	PIN_C22	SPI Slave Select Line for DAC	3.3-V LVTTL
SCLK_DAC	PIN_D22	SCLK for SPI clock input	3.3-V LVTTL
DIN_DAC	PIN_E22	SPI Data Line for DAC	3.3-V LVTTL

2.6 Controlling SDRAM

The board features 64MB of SDRAM with a single 64MB (32Mx16) SDRAM Chip. The chip has a 16-bit data line, control line, and address line directly connected to the FPGA. This chip uses the 3.3V LVCMOS signaling standard. The pin assignments for the SDRAM are listed in Table 2.6.

Table 2.6: SDRAM Pin Assignment

Signal Name	FPGA Pin No.	Description	I/O Standard
DRAM_ADDR0	PIN_U17	SDRAM Address [0]	3.3-V LVTTL
DRAM_ADDR1	PIN_W19	SDRAM Address [1]	3.3-V LVTTL
DRAM_ADDR2	PIN_V18	SDRAM Address [2]	3.3-V LVTTL
DRAM_ADDR3	PIN_U18	SDRAM Address [3]	3.3-V LVTTL
DRAM_ADDR4	PIN_U19	SDRAM Address [4]	3.3-V LVTTL
DRAM_ADDR5	PIN_T18	SDRAM Address [5]	3.3-V LVTTL
DRAM_ADDR6	PIN_T19	SDRAM Address [6]	3.3-V LVTTL
DRAM_ADDR7	PIN_R18	SDRAM Address [7]	3.3-V LVTTL
DRAM_ADDR8	PIN_P18	SDRAM Address [8]	3.3-V LVTTL
DRAM_ADDR9	PIN_P19	SDRAM Address [9]	3.3-V LVTTL
DRAM_ADDR10	PIN_T20	SDRAM Address [10]	3.3-V LVTTL
DRAM_ADDR11	PIN_P20	SDRAM Address [11]	3.3-V LVTTL
DRAM_ADDR12	PIN_R20	SDRAM Address [12]	3.3-V LVTTL
DRAM_DQ0	PIN_Y21	SDRAM Data [0]	3.3-V LVTTL
DRAM_DQ1	PIN_Y20	SDRAM Data [1]	3.3-V LVTTL
DRAM_DQ2	PIN_AA22	SDRAM Data [2]	3.3-V LVTTL
DRAM_DQ3	PIN_AA21	SDRAM Data [3]	3.3-V LVTTL
DRAM_DQ4	PIN_Y22	SDRAM Data [4]	3.3-V LVTTL
DRAM_DQ5	PIN_W22	SDRAM Data [5]	3.3-V LVTTL
DRAM_DQ6	PIN_W20	SDRAM Data [6]	3.3-V LVTTL
DRAM_DQ7	PIN_V21	SDRAM Data [7]	3.3-V LVTTL
DRAM_DQ8	PIN_P21	SDRAM Data [8]	3.3-V LVTTL
DRAM_DQ9	PIN_J22	SDRAM Data [9]	3.3-V LVTTL
DRAM_DQ10	PIN_H21	SDRAM Data [10]	3.3-V LVTTL
DRAM_DQ11	PIN_H22	SDRAM Data [11]	3.3-V LVTTL
DRAM_DQ12	PIN_G22	SDRAM Data [12]	3.3-V LVTTL
DRAM_DQ13	PIN_G20	SDRAM Data [13]	3.3-V LVTTL
DRAM_DQ14	PIN_G19	SDRAM Data [14]	3.3-V LVTTL
DRAM_DQ15	PIN_F22	SDRAM Data [15]	3.3-V LVTTL
DRAM_BA0	PIN_T21	SDRAM Bank Address [0]	3.3-V LVTTL
DRAM_BA1	PIN_T22	SDRAM Bank Address [1]	3.3-V LVTTL
DRAM_LDQM	PIN_V22	SDRAM Byte Data Mask [0]	3.3-V LVTTL
DRAM_UDQM	PIN_J21	SDRAM Byte Data Mask [1]	3.3-V LVTTL
DRAM_RAS_N	PIN_U22	SDRAM Row Address Strobe	3.3-V LVTTL
DRAM_CAS_N	PIN_U21	SDRAM Column Address Strobe	3.3-V LVTTL
DRAM_CKE	PIN_N22	SDRAM Clock Enable	3.3-V LVTTL
DRAM_CLK	PIN_L14	SDRAM Clock	3.3-V LVTTL
DRAM_WE_N	PIN_V20	SDRAM Write Enable	3.3-V LVTTL
DRAM_CS_N	PIN_U20	SDRAM Chip Select	3.3-V LVTTL